

Attorney Docket No. 42P8534C

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:)
Jin Yang) Examiner: Unassigned
Application No.: Unassigned) Art Unit: ***
Filed: Herewith)
For: SYMBOLIC MODEL CHECKING)
WITH DYNAMIC MODEL)
PRUNING)

)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the documents cited on that form. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Express Mail No: EV33586078US

Date of Deposit: September 17, 2003

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

- X 37 C.F.R. §1.97(b).
- _____ 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:
- _____ A statement pursuant to 37 C.F.R. §1.97(e) or
- _____ A check for \$180.00 for the fee under 37 C.F.R. § 1.17(p).
- _____ 37 C.F.R. §1.97(d). If so, then enclosed with this Information Disclosure Statement are the following:
- (1) A statement pursuant to 37 C.F.R. §1.97(e); and
- (2) A check for \$180.00 for the fee under 37 C.F.R. §1.17(p) for submission of the Information Disclosure Statement.

If there are any charges due, please charge them to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: September 17, 2003



Lawrence M. Mennemeier
Reg. No. 51,003

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025-1030
(408) 720-8300

Substitute for Form 1449A/PTO (Modified)			Attorney Docket No.: 42P8534C	Application Number: Unassigned		
Sheet 1 of 4			First Named Inventor: Jin Yang	Examiner: Unassigned		
			Filing Date: Herewith	Art Unit: Unassigned		
U.S. PATENT DOCUMENTS						
Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (If known)			
		5,119,318		Paradies et al.	06/02/1992	
		5,481,717		Gaboury	01/02/1996	
		5,469,367		Puri et al	11-21-1995	
		5,491,639		Filkorn	02-13-1996	
		5,594,656		Tamisier	01-14-1997	
		5,691,925		Hardin et al.	11/25/1997	
		5,754,454		Pixley et al	05-19-1998	
		5,768,498		Boigelot, et al	06-16-1998	
		5,905,977		Goubault	05-18-1999	
		5,937,183		Ashar et al	06-10-1999	
		6,026,222		Gupta et al	02-15-2000	
		6,035,109		Ashar et al	03-07-2000	
		6,086,626		Jain et al	07-11-2000	
		6,131,078		Plaisted	10-10-2000	
		6,148,436		Wohl	11-14-2000	
		6,185,516		Hardin et al	02-06-2001	
		6,209,120		Kurshan et al	03-27-2001	
		6,247,165		Wohl et al	06-12-2001	
		6,292,916		Abramovici et al	09-18-2001	
		6,301,687		Jain et al	10-09- 2001	
		6,308,299		Burch et al	10-23- 2001	
		6,321,186		Yuan et al	11-20- 2001	
		6,339,837		Li	01-15-2002	
		6,341,367	B1	Downing	01/22/2002	
Examiner Signature					Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Unique citation designation number. ²See attached Kinds of U.S. Patent Documents. ³Enter Office that issued the document, by the two-letter code (WIPO Standard S.3). For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. ⁴Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 42P8534C	Application Number: Unassigned
		First Named Inventor: Jin Yang	Examiner: Unassigned
Sheet 2 of 4		Filing Date: Herewith	Art Unit: Unassigned

OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
		BEREZIN, S. et al, "A Compositional Proof System for the Modal μ -Calculus and CCS," <i>Technical Report CMU-CS-97-105, Carnegie Mellon University</i> , January 15, 1997	
		BEREZIN, S. et al, "Model Checking Algorithms for the μ -Calculus," <i>Technical Report CMU-CS-96-180, Carnegie Mellon University</i> , September 23, 1996	
		BRADLEY, J. et al, "Compositional BDD Construction: A Lazy Algorithm," <i>Dept. of Computer Science, University of Bristol</i> , April 1998, pages 1-8.	
		BRYANT, R. E. et al, "Formal Hardware Verification by Symbolic Ternary Trajectory Evaluation," <i>28th ACM/IEEE Design Automation Conference</i> , Paper 24.2, 1991, pages 397-402	
		BRYANT, R. E., "Binary Decision Diagrams & Beyond," Tutorial at ICCAD '95, <i>Carnegie Mellon University</i> , 1995	
		BURCH, J. R. et al, "Representing Circuits More Efficiently in Symbolic Model Checking," <i>28th ACM/IEEE Design Automation Conference</i> , Paper 24.3, 1991, pages 403-407	
		BURCH, J. R. et al, "Sequential Circuit Verification Using Symbolic Model Checking," <i>27th ACM/IEEE Design Automation Conference</i> , Paper 3.2, 1990, pages 46-51	
		BURCH, J. R. et al, "Symbolic Model Checking for Sequential Circuit Verification," <i>IEEE Transactions on Computer-Aided Design for Integrated Circuits and Systems</i> , April 1994, pages 401-424	
		CAMPOS, S., "Real-Time Symbolic Model Checking for Discrete Time Models," <i>Technical Report CMU-CS-94-146, Carnegie Mellon University, Pittsburgh, PA</i> , May 2, 1994	
		CAMPOS, S., "Symbolic Model Checking in Practice," <i>IEEE Proceedings, XII Symposium on Integrated Circuits and System Design</i> , Oct 2, 1999, pages 98-101.	
		CHAN, W. et al, "Combining Constraint Solving and Symbolic Model Checking for a Class of Systems with Non-linear Constraints, <i>Computer Aided Verification, 9th International Conference, CAV '97 Proceedings (O. Grumberg, Editor)</i> , Lecture Notes in Computer Science 1254, pages 316-327, Haifa, Israel, June 1997. Springer-Verlag (Revised in December '98)	
		CHEN, Y. et al, "PBHD: An Efficient Graph Representation for Floating Point Circuit Verification," <i>Technical Report CMU-CS-97-134, Carnegie Mellon University</i> , May 1997	

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 42P8534C	Application Number: Unassigned
Sheet 3 of 4	First Named Inventor: Jin Yang	Examiner: Unassigned
	Filing Date: Herewith	Art Unit: Unassigned

OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
		CHEUNG, S. et al, "Checking Safety Properties Using Compositional Reachability Analysis," <i>ACM Transactions on Software Engineering and Methodology</i> , Vol. 8, No. 1, January 1999, pages 49-78	
		CHIODO, M. et al, "Automatic Compositional Minimization in CTL Model Checking," <i>Proceedings of 1992 IEEE/ACM International Conference on Computer-Aided Design</i> , November, 1992, pages 172-178	
		CHOU, C., "The Mathematical Foundation of Symbolic Trajectory Evaluation," <i>International Conference on Computer-Aided Verification(CAV'99)</i> , Trento, Italy, July 1999 pp. 196-207, Proceedings of CAV'99, Lecture Notes in Computer Science #1633 (Editors: Nicolas Halbwachs & Doron Peled), Springer-Verlog, 1999	
		CLARKE, E. et al, "Another Look at LTL Model Checking," <i>Technical Report CMU-CS-94-114</i> , Carnegie Mellon University, February 23, 1994	
		CLARKE, E. et al, "Combining Symbolic Computation and Theorem Proving: Some Problems of Ramanujan," <i>Technical Report CMU-CS-94-103</i> , Carnegie Mellon University, January 1994	
		CLARKE, E. M. et al, "Formal Methods: State of the Art and Future Directions," <i>ACM Computing Surveys</i> , Vol. 28, No. 4, December 1996, pages 626-643	
		CLARKE, E. M. et al, "Model Checking and Abstraction," <i>Proceedings of the 19th ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages</i> , February 1992, pages 343-354	
		CLARKE, E. M. et al, "Model Checking and Abstraction," <i>ACM Transactions on Programming Languages and Systems</i> , Vol. 16, No. 5, September 1994, pages 1512-1542	
		GRUMBERG, O., "Model Checking and Modular Verification," <i>ACM Transactions On Programming Languages and Systems</i> , Vol. 16, No. 3, May 1994, pages 843-871	
		Hojati, R. et al, "Early Quantification and Partitioned Transition Relations," <i>Proceedings, IEEE International Conference on Computer Design: VLSI in Computers and Processors</i> , Oct. 9, 1996, pages 12-19	
		JACKSON, D., "Exploiting Symmetry in the Model Checking of Relational Specifications," <i>Technical Report CMU-CS 94-219</i> , Carnegie Mellon University, December 1994	

Examiner Signature	Date Considered
--------------------	-----------------

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 42P8534C	Application Number: Unassigned
Sheet 4 of 4		First Named Inventor: Jin Yang	Examiner: Unassigned
		Filing Date: Herewith	Art Unit: Unassigned

OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
		JAIN, A. et al, "Verifying Nondeterministic Implementations of Determinist Systems," <i>Lecture Notes in Computer Science, Formal Methods in Computer Aided-Design</i> , pp. 109-125, November 1996	
		JAIN, A., "Formal Hardware Verification by Symbolic Trajectory Evaluation," <i>Carnegie Mellon University Ph.D. Dissertation</i> , July 1997	
		JAIN, S. et al, "Automatic Clock Abstraction from Sequential Circuits," <i>Proceedings of the 32nd ACM/IEEE Conference on Design Automation</i> , January 1995	
		JHA, S. et al, "Equivalence Checking Using Abstract BBDs," <i>Technical Report CMU-CS-96-187, Carnegie Mellon University, Pittsburgh, PA</i> , October 29, 1996	
		KERN, C. et al, "Formal Verification In Hardware Design: A Survey," <i>ACM Transactions on Design Automation of Electronic Systems</i> , Vol. 4, No. 2, April 1999, pages 123-193	
		KURSHAN, R. et al, "Verifying Hardware in its Software Context," <i>Proceedings of the 19th ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages</i> , February 1992, pages 742-749	
		NELSON, K. L. et al, "Formal Verification of a Superscalar Execution Unit," <i>34th Design Automation Conference</i> , June 1997	
		TUYA, J. et al, "Using a Symbolic Model Checker for Verify Safety Properties in SA/RT Models," <i>Proceeding of the 5th European Software Engineering Conference, Lecture Notes in Computer Science</i> , Vol. 989, Springer-Verlag, Berlin, 1995, pages 59-75	
		VELEV, M. N., "Efficient Modeling of Memory Arrays in Symbolic Simulations," <i>Proceedings of Computer-Aided Verification</i> , June 1997	
		WING, J. M. et al, "A Case Study in Model Checking Software Systems," <i>Technical Report CMU-CS-96-124, Carnegie Mellon University, Pittsburgh, PA</i> , April 1996	
		YEH, W. et al, "Compositional Reachability Analysis Using Process Algebra," <i>28th ACM/IEEE Design Automation Conference</i> , 1991	
		Zhang Z., "An Approach to Hierarchy Model Checking via Evaluating CTL Hierarchically," <i>IEEE Proceedings of the Fourth Asian Test Symposium</i> , Nov. 24, 1995, pages 45-49.	

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.